AXIS ETRAX 100

High-Performance Ethernet Peripheral Controller

Peripheral Controller

Designed to meet manufacturers' demands for low cost, easy implementation and superior network performance, the ETRAX 100 is Axis' fifth-generation optimized system-on-a-chip solution for putting peripherals on the network. The ETRAX 100 was developed using 0.35µm ASIC technology with the best price/performance ratio available today. It is a member of the ETRAX RISC chip family with more than 1 million units shipped, making it the most widely used network-attached architecture. Applications include networked printers, copiers, multi-function peripherals and network-attached storage.

RISC CPU Delivers Exceptional Performance with Low Power Consumption

The innovative 100 MIPS 32-bit RISC design delivers compact code and exceptional price/performance at low power consumption. An 8-kbyte on-chip cache helps to take full advantage of the CPU performance. An optimized C/C++ compiler is available.

Network Controller Simplifies Design and Improves Throughput

The on-chip Fast Ethernet controller simplifies the hardware design as most logical and physical connectivity is on one chip. The controller also provides excellent network throughput and supports zero copy network protocol stacks.

Feature-rich I/O Makes It Suitable for a Wide Range of Applications

Intelligent DMA-driven ports provide cost-effective connections to devices with SCSI-2, SCSI-3, EIDE/ATA-2, parallel, and serial interfaces. The ETRAX 100 has a DMA data transfer rate of up to 200 Mbytes/second, which supports the most demanding of network applications today and in the future.

Memory Bus Interfaces Lower Product Design Costs

The ETRAX 100 has 2 Gigabytes of address space and supports SRAM, DRAM, EPROM, EEPROM, and Flash PROM without external logic, which lowers cost and makes design easy.

Network Bootstrap Provides Extra Reliability for Thin Servers

The ETRAX 100 features a patent-pending network bootstrap function which enables ETRAX 100-based products to be booted remotely over the network, even if they have no executable program code in memory.

Management Tools and Multiple OS Support Complete the Solution

ETRAX is a part of Axis' ThinServer™ Technology, which consists of protocol stacks, server software, "thin" versions of real-time operating systems and Web-based management tools. Axis' core architecture supports open standards such as SLP, Sun's Jini and the Ericsson-led "Bluetooth" wireless initiative.

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Peripheral Controller

Technical Specifications

32-BIT RISC CPU

RISC CPU with 32-bit data and address format. 15 general 32-bit registers. Instruction set optimized for compact code and high speed with 16/32-bit bus width. Peak performance of 100 MIPS.

CACHE MEMORY

8 kbyte on-chip direct mapped unified instruction/data cache memory.

ETHERNET CONTROLLER

Ethernet controller supporting 100 Mbit and 10 Mbit (compatible with IEEE 802.3 and Fast Ethernet standards). ETRAX 100 interfaces to 100 Mbit/10 Mbit MII and 10 Mbit NS DP8391A Serial Network Interface.

DMA

Ten internal DMA channels provide handling of data within the chip as well as to and from external units. The channels are unidirectional, five in each direction. Two channels for external I/O are provided. Each of those uses two internal channels, one in each direction.

Eight of the DMA channels have a 64 byte FIFO. The two channels used for serial port 1 do not have FIFOs.

DMA-DRIVEN PORTS

The ten DMA channels can be configured for connecting to SCSI, EIDE/ATA-2, parallel ports, serial ports, and memory. These applications are multiplexed on the same pins. Combinations where the applications do not overlap are allowed. There are two additional serial ports that are always available. Channel usage is decided by setting internal registers.

SCSI AND EIDE/ATA-2

Initiator (host) mode SCSI controller that supports either two 8-bit wide or one 16-bit wide SCSI interface. Synchronous and asynchronous data transfer are supported. External bus drivers are required. The disk interface can also be configured as an EIDE/ATA-2 port with support for up to 8 disk drives. The SCSI ports and the EIDE/ATA-2 interface are multiplexed on the same pins as the parallel ports and two of the serial ports. Configuration is decided by internal registers.

TWO PARALLEL I/O PORTS

The ports can be configured to support various parallel printer protocols, including

- IBM XT/AT compatible Centronics
- IBM PS/2 compatible Centronics
- Hewlett-Packard Fast Mode
- IBM Fastbyte
- Bitronics, compatible with IEEE 1284 and HP Boise specifications (modes byte, nibble, and ECP)

FOUR SERIAL PORTS

Supports baud rates from 300 up to 1843200 baud and a non-standard baud rate of 6.25 Mbaud. Two of the ports are constantly available and two are multiplexed with other I/O. Baud rate and operating mode can be set independently for each channel. Operating modes:

- Odd, even or no parity
- 7 or 8 bits
- 1 or 2 stop bits
- HW or SW handshake

BOOTSTRAP PROGRAM DOWNLOAD

Support for initial loading to internal cache memory from serial port and network. Code, loaded to cache, can be designed to enable download of program to initially empty Flash PROM or other external memory.

BUS INTERFACE

16-bit/32-bit bus interface supporting SRAM, DRAM, EPROM, parallel EEPROM, and FlashPROM without external logic.

- Six internally decoded chip select outputs.
- Six additional chip select outputs are multiplexed with other I/O functions.
- Direct interface for four DRAM banks. Fast Page mode access and EDO access supported.

A 25-bit address bus, using bits 1 to 25, gives an address space of 64 MB per memory bank. The bus width and number of waitstates can be configured individually for EPROM, SRAM and DRAM banks. Maximum bus cycle frequency is 50 MHz.

TIMERS

- Two programmable timers. Programmable range from 160 ns to 850 ms
- Watchdog timer

GENERAL PURPOSE PORTS

Two general purpose ports that each contain 8 bits of individually controlled I/O-pins

CLOCK GENERATOR

Internal 100 MHz operating frequency, generated by a PLL from an external 20 MHz clock signal.

INTERRUPT CONTROL

ETRAX 100 provides vectorized interrupt, internal (I/O ports, network interface, DMA, and timer) and external (IRQ and NMI).

DEVELOPMENT TOOLS

C, C++ compiler: Cross compiler running on SUN SPARC platform. (Based on GNU CC from Free Software Foundation.)

Logic Analyzer support: Specially designed logic analyzer from Axis Communications enables tracing of code execution from internal cache.

PACKAGE

256-pin Plastic Ball Grid Array package, 27x27x2.15mm.

POWER

Power dissipation (outputs open): 510mW typ., 800 mW max.

OPERATING CONDITIONS

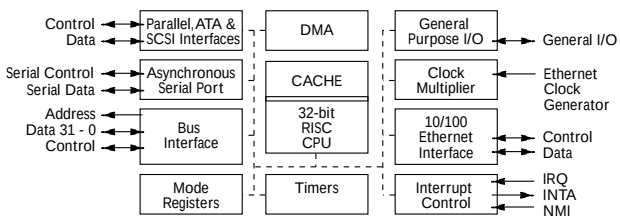
Supply voltage: 3.0 - 3.6V

Ambient temperature range: 0 - 70° C

THINSERVER TECHNOLOGY

The AXIS ETRAX 100 is a component of Axis' ThinServer Technology. This technology is comprised of thin versions of the most popular network operating systems, Web management tools and the ETRAX 32-bit RISC processor — based on open architecture and streamlined and optimized for device connectivity independent of any file servers.

Functional Blocks



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