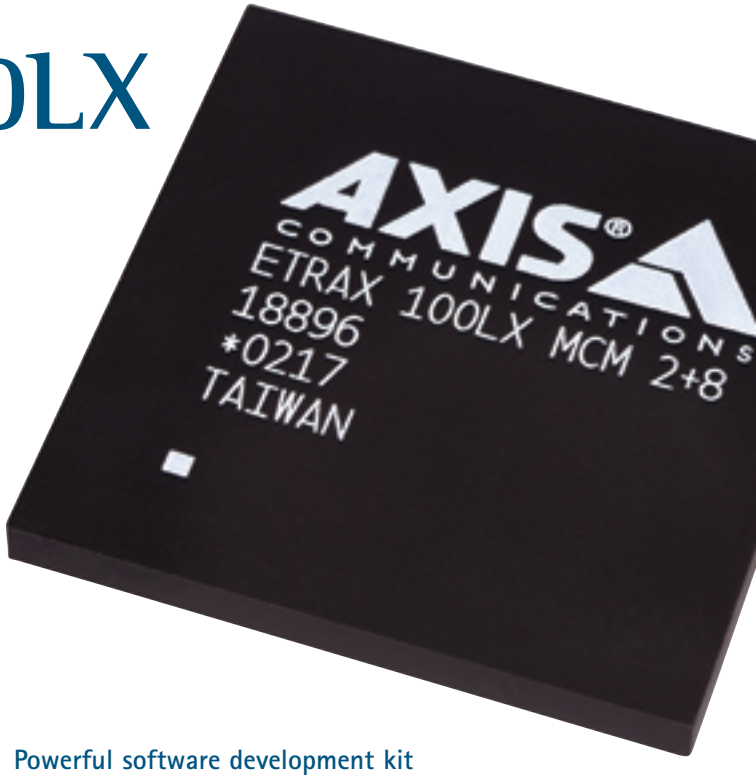
AXIS ETRAX 100LX MCM 2+8

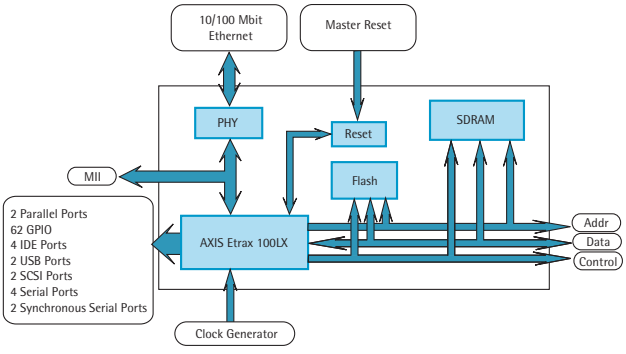
The complete Linux computer in a single multi-chip module



The AXIS ETRAX 100LX MCM integrates the most common components used within a standard ETRAX hardware design, such as 2MB Flash, 8MB SDRAM and Ethernet Transceiver, into a single multi-chip module (MCM). Optimal miniaturization and easier integration into your target system design are amongst the many potential benefits offered by its modular system architecture.

Reducing development lead times

With most of the timing-sensitive components integral in its design, the AXIS ETRAX 100LX MCM eliminates the time-consuming effort required for developing reliable system hardware. For you as a system designer, the AXIS ETRAX 100LX MCM provides a stable hardware platform that leaves you free to focus on your product design. Cutting development lead times significantly, you can now design your system in days rather than weeks!



Powerful software development kit

The SDK for the AXIS ETRAX 100LX family is based on the standard Linux 2.4 kernel, which allows you to port applications available for standard PC Linux quickly and easily. Including a Memory Management Unit (MMU), the ETRAX processor provides memory protection and 100% source code compatibility with common Linux applications.

- Powerful integrated SoC based on AXIS ETRAX 100LX
- Designed for running Linux 2.4, includes an MMU
- Low power consumption
- 2MB Flash and 8MB SDRAM integrated
- 10/100 Mbit Ethernet, including integrated transceiver
- Several I/O options e.g. Ethernet, RS-232/485, USB, IDE, SCSI, Parallel, GPIO...
- No license fees
- Extensive documentation and reference designs available on http://developer.axis.com

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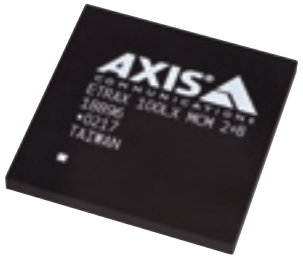
Technical Specification - AXIS ETRAX 100LX MCM 2+8



Component Specification

The multi-chip-module contains the following components:

AXIS ETRAX 100LX:

- The powerful AXIS ETRAX 100LX (also available as a separate component) is presented separately below. Please see the AXIS ETRAX 100 LX datasheet for full details about this component

SDRAM:

- 8MB SDRAM
- 16-bit interface
- More RAM can be added externally to enable a 32-bit interface

FLASH Memory:

- 2MB Integrated Flash
- More FLASH can be added externally

Ethernet Transceiver:

- 10/100 Mbit Ethernet PHY
- Supports full duplex mode
- Autosensing speed and duplex mode

Other components:

- 50 passive components (resistors and capacitors)
- Reset circuitry

Package

- 256-pin Plastic Ball Grid Array package, 27 x 27 x 2.76 mm

Power

- Power dissipation (outputs open): 900 mW typical 1100 mW max

Operating Conditions

- Supply voltage: 3.0 - 3.6V
- Ambient temperature range: 0 - 70°C

Software and Development Tools

- The Linux kernel 2.4 or subsequent for AXIS ETRAX 100LX, including device drivers for all ETRAX ports, is available for download from the Axis developer Web site http://developer.axis.com

Technical Specification - AXIS ETRAX 100LX

32-Bit RISC CPU

- RISC CPU with a 32-bit data and address format. 15 general 32-bit registers. Instruction set optimized for compact code and high speed with 16/32-bit bus width. Runs on a 100 MHz clock. User and Supervisor mode for restricted access and selection of appropriate address mapping by the MMU

Memory Management Unit (MMU)

- MMU featuring 4 GB of virtual uniformed address space for each user process with address space protection so that user applications do not have access to data of other applications, or the operating system

Ethernet Controller

- Ethernet controller supporting 100 Mbit and 10 Mbit (compatible with IEEE 802.3 and Fast Ethernet standards). AXIS ETRAX 100LX interfaces to Media Independent Interface and Serial Network Interface

Direct Memory Access (DMA)

- 10 DMA channels each with a 64 byte FIFO for low latency and high throughput data transfer to and from internal and external units (200 MBytes/sec total peak bandwidth to share between the 10 DMA channels)

4 Asynchronous Serial Ports*

- Internal baud rate programmable from 48 Hz to 1.5625 MHz, or external baud rate up to 3.125 MHz. Fixed baud rates from 300 Hz to 1843.2 kHz, and a non-standard baud rate at 6.25 MHz

2 Synchronous Serial Ports*

- Master or Slave synchronous serial mode with codec clock between 32 kHz and 4.096 MHz

2 USB Ports*

- Universal Serial Bus 1.1 Host and Device mode operation

2 Parallel I/O Ports*

- The ports can be used through register access or internal DMA access, and can be configured to support various protocols

ATA*

- Configuration of up to 4 ATA ports for up to 8 IDE disk drives.

General Purpose Ports*

- Two general-purpose ports that each contain 8 bits of individually controlled I/O ports. In addition to this, every non-used pin on the other I/O interfaces may be used for general purpose I/O, enabling up to 62 GPIO signals

SCSI*

- Initiator (host) mode SCSI controller that supports either two 8-bit wide, or one 16-bit wide, SCSI interface

Bootstrap Program Download

- Support for initial loading to internal cache memory from parallel port, serial port and network. Code, loaded to cache, can be designed to enable download of program to initially empty Flash PROM or other external memory

Timers and Watchdog

- Two eight-bit timers with programmable clock from 381 Hz to 12.5 MHz. Fixed timer clocks from 300 Hz to 6.25 MHz. Additional watchdog timer

Clock Generator

- Internal 100 MHz operating frequency, generated by a PLL from an external 20 MHz clock signal

Interrupt Control

- Vectorized interrupt; internal (I/O ports, network interface, DMA and timer) and external (IRQ and NMI)

*Two of the asynchronous serial ports, the synchronous serial ports, parallel, USB, ATA and SCSI are multiplexed on the same pins and are not available all at the same time. Two of the serial ports are located on dedicated pins and are always available.

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For more information visit our Web site: **developer.axis.com**

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